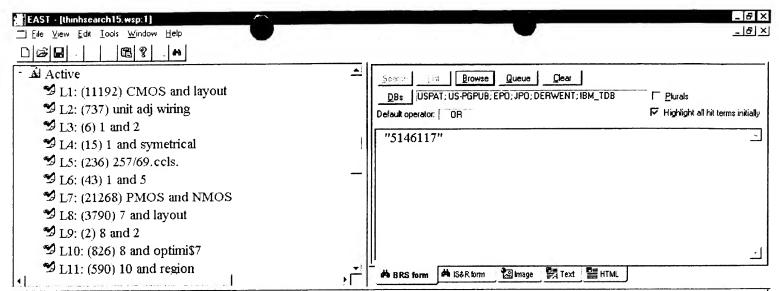
L Number		Search Text CMOS and layout	DB USPAT; US-PGPUB;	Time stamp 2903/03/13 08:57
			EPO; JPO; DERWENT; IBM_TDB	
2	737	unit adj wiring	USPAT: US-PGPUB; EPO; JPO;	2003/03/13 08:58
			DERWENT. IBM_TDB USPAT;	2003/03/13 09:00
3	6	(CMOS and layout) and (unit adj wiring)	US-PGPUB. EPO; JPO;	2003/03/13 07:00
4	737 6 15 236 43 21268 3790 2	(CMOS and layout) and symetrical	DERWENT, IBM_TDB USPAT:	2003/03/13 09:15
			US-PGPUB, EPO: JPO: DERWENT,	
5	236	257/69.ccls.	IBM_TDB USPAT; US-PGPUB,	2003/03/13 09:16
			EPO; JPO; DERWENT, IBM_TDB	2002/02/12 00:28
6	43	(CMOS and layout) and 257/69.ccls.	USPAT; US-PGPUB, EPO; JPO;	2003/03/13 09:38
7	21268	PMOS and NMOS	DERWENT. IBM_TDB USPAT; US-PGPUB.	2003/03/13 09:38
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8	3790	(PMOS and NMOS) and layout	USPAT: US-PGPUB, EPO, JPO;	2003/03/13 09:39
0	2	(m) (CC and N) (MOC) and lowerth and (unit adi wiring)	DERWENT, IBM_TDB USPAT;	2003/03/13 09:45
9	2	((PMOS and NMOS) and layout) and (unit adj wiring)	US-PGPUB. EPO, JPO; DERWENT.	2003/03/13 0 1.13
10	826	((PMOS and NMOS) and layout) and optimi\$7	IBM_TDB USPAT: US-PGPUB.	2003/03/13 09:50
			EPO, JPO; DERWENT, IBM_TDB	
11	590	(((PMOS and NMOS) and layout) and optimi\$7) and region	USPAT; US-PGPUB, EPO; JPO;	2003/03/13 09:52
			DERWENT: IBM_TDB USPAT;	2003 03.13 09:52
12	1351406	"12" and metal	US-PĞPUB; EPO; JPO; DERWENT;	2003 V3-13 V7-32
			IBM_TDB	

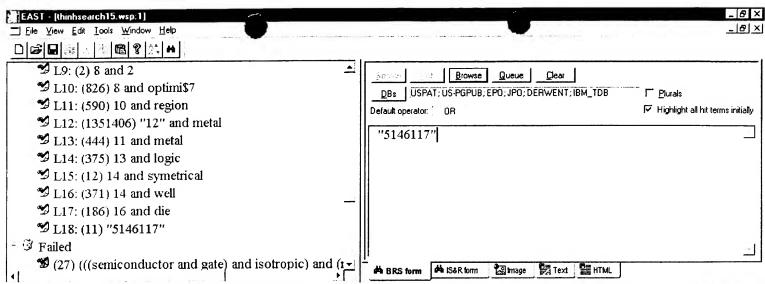
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15	12	((((((PMOS and NMOS) and layout) and optimi\$7) and region) and metal) and logic) and symetrical	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2003/03/13 09:55
16	371	((((((PMOS and NMOS) and layout) and optimi\$7) and region) and metal) and logic) and well	USPAT: US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2003/03/13 09:57
17	186	(((((((PMOS and NMOS) and layout) and optimi\$7) and region) and metal) and logic) and well) and die	USPAT: US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 11:46
18	11	"5146117"	USPAT: US-PGPUB: EPO; JPO; DERWENT; IBM_TDB	2003/03/13 11:46



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	
1	_		US 6294816 B1	20010925	10	Secure integrated circuit	257/368	257/369;	
	<u> </u>	1						257/659;	
2	┍	_	US 6255908 B1	20010703			330/149	330/145	
	,,,	1				digitally controlled amplitude and pha		40.	
3	_	_	US 6173436 B1	20010109	10	Standard cell power-on-reset circuit	716/19	716/1;	
	'	•						716/11	
4	_	Г	US 6064110 A	20000516	12	Digital circuit with transistor geometry	257/652	257/204;	
		٠.				and channel stops providing camoufl		257/376;	
5	_	_	US 5973375 A	19991026	16	Camouflaged circuit structure with	257/399	257/648;	1
	'	'				step implants		257/E27.009;	
6	_	г	US 5930663 A	19990727		Digital circuit with transistor geometry	438/598	257/390;	
	'					and channel stops providing camoufl		257/E27.009;	- 1
7	_	_	US 5866933 A	19990202	10	Integrated circuit security system and	257/368	257/369;	-1
	•	•				method with implented interconnection		757/650.	ان
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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRe	ef 🗅
1	_	_	US 6294816 B1	20010925	10	Secure integrated circuit	257/368	257/369;	
		1						257/659;	
2	U	_	US 6255908 B1	20010703	18		330/149	330/145	
	1*	•				digitally controlled amplitude and pha			
3	_	_	US 6173436 B1	20010109	.10	Standard cell power-on-reset circuit	716/19	716/1;	
	1	•						716/11	
4	Г	г	US 6064110 A	20000516	12	Digital circuit with transistor geometry	257/652	257/204;	لــ
	•	•				and channel stops providing camoufl		257/376;	
5	_	г	US 5973375 A	19991026	16	Camouflaged circuit structure with	257/399	257/648;	
	•	•				step implants		257/E27.009;	
б	_	Г	US 5930663 A	19990727		Digital circuit with transistor geometry	438/598	257/390;	
	•	•				and channel stops providing camoufl		257/E27.009;	
7	Г	Г	US 5866933 A	19990202	10	Integrated circuit security system and	257/368	257/369;	-1
		•				method with implement interconnection		257/650-	ن ر

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